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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,849	07/10/2003	Hayato Nakanishi	116506	9980

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EXAMINER	
TRAN, HENRY N	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,849	NAKANISHI, HAYATO	
	Examiner	Art Unit	
	Henry N. Tran	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment received December 30, 2005 has been fully considered; and this Office action is in response thereto.

Claims 1-13 remain pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new grounds of rejection provided hereinafter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 and 6-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada et al (U.S. Patent No. 6,690,110, hereinafter referred to as "Yamada").

5. Regarding claim 1, Yamada, Fig. 3A, 3B, 4 and 5B, teaches an electro-optical device comprising: a substrate (10); a plurality of first electrodes (6) disposed in an effective region (300) on a substrate; a second electrode (25) acting as a common electrode for a plurality of the first electrodes; a plurality of electro-optical elements (EM) each disposed between the second electrode and the corresponding first electrodes; first wiring lines (WD1, WD2 and VL) for applying power-supply voltages to the first electrodes; and a second wiring line (WD3 and

WD4), connected to the second electrode, lying between the effective region (300) and at least one of a plurality of sides of the substrate (the bottom region defined by the cathode forming region 25 and the sealing region 250), wherein the area of the second wiring line disposed on the substrate is larger than the total area of parts of the first wiring lines, the parts being disposed outside the effective region on the substrate (Fig. 3A, Yamada shows area WD3 + WD4 > WD1 + WD2).

6. Regarding claim 2, Yamada, Fig. 3A, shows that the second wiring line has a portion having a width larger than that of the first wiring lines (WD4 > WD1 or WD2).

7. Regarding claim 3, Yamada, Fig. 3A, shows that the width of the entire second wiring line is larger than that of the first wiring lines (i.e., WD3 + WD4 > WD1 + WD2).

8. Regarding claim 6, Yamada, Fig. 3A, shows that the substrate (10) has a dummy region disposed between the effective region (300) and at least one of a plurality of sides of the substrate (the region which is outside of the effective region (300) but inside the seal region (250)), and the first wiring lines and the second wiring line are arranged between the dummy region and at least one of a plurality of sides of the substrate.

9. Regarding claim 7, Yamada, Fig. 3A, teaches the second electrode (25) covers at least the effective region and the dummy region.

10. Regarding claim 8, Yamada, Fig. 6A, shows that a connection (L5) between the second wiring line (WD3 and WD4) and the second electrode (25) lies between the effective region (300) and at least three of a plurality of sides of the substrate.

11. Regarding claim 9, Yamada, Figs. 3A and 4, shows a plurality of the first electrodes (WD1, WD2, and VL) are each included in corresponding pixel electrodes arranged in the

effective region and each include a plurality of control lines (GL and DL) for transmitting signals for controlling the pixel electrodes (6), and a plurality of the control lines are arranged such that each control line and at least one of the first wiring lines and the second wiring line do not cross on the substrate.

12. Regarding claim 10, Yamada, Fig. 4, shows that the control lines each include corresponding scanning lines (GL) for transmitting scanning signals to the corresponding pixel electrodes and also each include corresponding data lines (DL) for transmitting data signals to the corresponding pixel electrodes.

13. Regarding claim 11, Yamada, Fig. 5B, shows the electro-optical elements (EM) each include corresponding hole injection/transport layers (21, 22 and 24) and corresponding light-emitting layers (23) containing an organic electroluminescent material, each hole injection/transport layer and light-emitting layer being stacked.

14. Regarding claim 12, Yamada further teaches that an electronic apparatus, such as an electroluminescent display device, comprising an electro-optical device according to claim 1; see col. 13, lines 39-45.

15. Regarding claim 13, which comprises similar claimed elements and limitations of claim 1, and is therefore rejected on the same basis set forth in claim 1 discussed above.
(Note that, Yamada, Fig. 6A, shows, the area of the second wiring line, i.e., WD3 + WD4 + 2L5, disposed on the substrate (10) is larger than the total area of parts of the first wiring lines, the parts being disposed outside the effective region on the substrate, i.e., Wd1 +WD2; wherein, WD3 + WD4 + 2L5 > Wd1 +WD2).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yamazaki et al (U.S. Patent No. 6,825,820, hereinafter referred to as "Yamazaki").

Yamada teaches generally all except for the: (i) a plurality of the electro-optical elements include a plurality of types of elements classified depending on the color of light emitted from the light-emitting layers, and the first wiring lines are arranged depending on the color of emitted light; and (ii) the width of the second wiring line disposed outside the effective region is larger than the width of part of one of the first wiring lines arranged depending on the type of the electro-optical elements, the part being disposed outside the effective region, the one being the widest of the first wiring lines.

Yamazaki, Figs. 1A, 1B, 14A and 14B, teaches, a plurality of types of elements (106) classified depending on the color of light emitted from the light-emitting layers (RGB EL elements); and the first wiring lines, 107r, 107b and 107g, are arranged depending on the color of emitted light; see col. 5, line 41 to col. 6, line 43.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the Yamazaki RGB EL elements structure with wiring width selection with the Yamada wiring arrangements because this would adjust the potentials needed for the

pixels of each of the colors to maintain a balance in the light emitting brightness of the color display device; see Yamazaki, col. 3, lines 6-9.

Claims 4 and 5 are dependent upon the base claim 1, and are therefore rejected on the same reasons set forth in claim 1, and by the reasons discussed above.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry N. Tran whose telephone number is 571-272-7760. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Henry N. Tran

Henry N Tran
Primary Examiner
Art Unit 2629

HT
4/6/06